Amendments to the Claims:

Please cancel claims 1-40, 42-49, 57-60, 68, 70, 75, 80, 84, 88-126 without prejudice or disclaimer. This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1-40. (Cancelled)

41. (Original) A data storage system comprising:

a reference array including a plurality of reference cells, a plurality of bit lines, a plurality of control gate lines, and at least one common line, each reference cell is configurable to store one of 2^N values, where N is at least two or greater;

a plurality of local sense amplifiers, each of said plurality of local sense amplifiers being coupled to a corresponding subset of said plurality of reference cells and being selectively coupled to said bitlines;

a plurality of global bitlines, each local sense amplifier being coupled to one of said plurality of global bitlines; and

a plurality of global sense amplifiers, each global sense amplifier being coupled to a group of said global bitlines to generate an output signal indicative of a reference signal corresponding to the selected reference cell.

42-49. (Cancelled)

50. (Original) A data storage system comprising:

a plurality of memory arrays, each memory array including a plurality of memory cells, a plurality of bit lines, a plurality of control gate lines, and at least one common line, each memory cell is configurable to store one of 2^N values, where N is two or greater;

at least one memory decoder coupled to the memory arrays, each memory decoder configured to provide bias signals to selected ones of the plurality of memory cells;

a reference array operatively coupled to the memory arrays and configurable to provide reference signals used for programming and reading the selected ones of the plurality of memory cells, the reference signals being stored in a real time relationship to receiving programming signals corresponding to said reference signals;

a plurality of local sense amplifiers, each of said plurality of local sense amplifiers being coupled to a corresponding subset of said plurality of memory cells and being selectively coupled to said bit lines;

a plurality of global bit lines, each local sense amplifier being coupled to one of said plurality of global bitlines; and

a plurality of global sense amplifiers, each global sense amplifier being coupled to a group of said global bitlines and said reference array to generate an output signal indicative of the comparison between a voltage detected in a selected memory cell and a reference signal.

51. (Original) The data storage system of claim 50 wherein the global sense amplifier capacitively detects a voltage on one of said global bitlines and capacitively detects one of said reference signals and generates an output signal indicative of the comparison between said detected voltage and a selected reference cell and said detected reference signal.

52. (Original) The data storage system of claim 50 wherein the global sense amplifier includes a circuit for coupling inputs of the global sense amplifier to the output signal in response to an autozero signal.

53. (Original) A data storage system comprising:

a plurality of reference memory subarrays, each reference memory subarray comprising a plurality of reference memory cells, each memory cell being configurable to store one of a plurality of reference signal levels; and

a plurality of reference sense amplifiers, each reference sense amplifier being selectively coupled to a corresponding subarray to capacitively sense content of a memory cell.

54. (Original) A data storage system comprising:

a plurality of memory arrays, each memory array including a plurality of memory cells, a plurality of bit lines, a plurality of control gate lines, and at least one common line, each memory cell is configurable to store one of 2^N values, where N is two or greater;

at least one memory decoder coupled to the memory arrays, each memory decoder configured to provide bias signals to selected ones of the plurality of memory cells;

a reference array operatively coupled to the memory arrays and configurable to provide reference signals used for programming and reading the selected ones of the plurality of memory cells, the reference signals being stored in a real time relationship to receiving programming signals corresponding to said reference signals;

a plurality of local sense amplifiers, each of said plurality of local sense amplifiers being coupled to a corresponding subset of said plurality of memory cells and being selectively coupled to said bit lines;

a plurality of global bit lines, each local sense amplifier being coupled to one of said plurality of global bitlines; and

a plurality of global sense amplifiers, each global sense amplifier being coupled to a group of said global bitlines to capacitively detect a voltage on one of said global bitlines and to said reference array to capacitively detect one of said reference signals, and to generate an output signal indicative of the comparison between said detected voltage in a selected memory cell and said detected reference signal.

55. (Original) A data storage system comprising:

a plurality of reference memory subarrays, each reference memory subarray comprising a plurality of reference memory cells, each reference memory cell being configurable to store one of a plurality of reference signal levels; and

a plurality of reference sense amplifiers, each sense reference amplifier being selectively coupled to a reference memory subarray to sense with autozero content of a reference memory cell.

56. (Original) A data storage system comprising:

a plurality of memory arrays, each memory array including a plurality of memory cells, a plurality of bit lines, a plurality of control gate lines, and at least one common line, each memory cell is configurable to store one of 2^N values, where N is two or greater;

at least one memory decoder coupled to the memory arrays, each memory decoder configured to provide bias signals to selected ones of the plurality of memory cells;

a reference array operatively coupled to the memory arrays and configurable to provide reference signals used for programming and reading the selected ones of the plurality of memory cells, the reference signals being stored in a real time relationship to receiving programming signals corresponding to said reference signals;

a plurality of local sense amplifiers, each of said plurality of local sense amplifiers being coupled to a corresponding subset of said plurality of memory cells and being selectively coupled to said bit lines;

a plurality of global bit lines, each local sense amplifier being coupled to one of said plurality of global bitlines; and

a plurality of global sense amplifiers, each global sense amplifier being coupled to a group of said global bitlines to capacitively detect a voltage on one of said global bitlines and said reference array to capacitively detect one of said reference signals to generate an output signal indicative of the comparison between said detected voltage in a selected memory cell and said detected reference signal, and including a circuit to equalize inputs and the output of the global sense amplifier in response to an autozero signal.

57-60. (Cancelled)

61. (Original) A data storage system comprising:

a plurality of memory arrays, each memory array including a plurality of memory cells, a plurality of bit lines, a plurality of control gate lines, and at least one common line, each memory cell is configurable to store one of 2^N values, where N is two or greater;

at least one memory decoder coupled to the memory arrays, each memory decoder configured to provide bias signals to selected ones of the plurality of memory cells;

a plurality of local sense amplifiers, each of said plurality of local sense amplifiers being coupled to a corresponding subset of said plurality of memory cells and being selectively coupled to said bit lines;

a plurality of global bit lines, each local sense amplifier being coupled to one of said plurality of global bitlines;

a plurality of global sense amplifiers, each global sense amplifier being coupled to a group of said global bitlines to generate an output signal indicative of the comparison between a voltage detected in a selected memory cell and one of a plurality of reference signals, and including a circuit to equalize inputs and the output of the global sense amplifier in response to an autozero signal; and

a circuit to compare the output signal from one of said global sense amplifiers corresponding to a selected memory cell and said detected reference signals from said reference array to verify contents of said selected memory cell and programming said selected memory cell in the event the comparison indicates content of said selected memory cell does not match said detected reference signals.

62. (Original) The data storage system of claim 61 further comprising a reference array operatively coupled to the memory arrays and configurable to provide stored reference signals used for programming and reading the selected ones of the plurality of memory cells, the stored reference signals corresponding to said detected plurality of reference signals.

63. (Original) A data storage system comprising:

a plurality of memory arrays, each memory array including a plurality of memory cells, each memory cell is configurable to store one of 2^N values, where N is two or greater;

at least one memory decoder coupled to the memory arrays, each memory decoder configured to provide bias signals to selected ones of the plurality of memory cells;

a reference array operatively coupled to the memory arrays and configurable to provide reference signals used for programming and reading the selected ones of the plurality of memory cells;

a plurality of local sense amplifiers, each of said plurality of local sense amplifiers being coupled to a corresponding subset of said plurality of memory cells;

a plurality of global sense amplifiers, each global sense amplifier being coupled to a group of local sense amplifiers and said reference array to generate an output signal indicative of the comparison between a voltage detected in a selected memory cell and a reference signal; and

a circuit to compare the output signal from one of said global sense amplifiers corresponding to a selected memory cell and one of said reference signals from said reference array and determining whether said output signal is within a predetermined relationship of said one of said reference signals during a programming, erase or reading of said selected memory cell and setting a flag to indicate whether a predetermined relationship is determined.

64. (Original) A data storage system comprising:

a plurality of memory arrays, each memory array including a plurality of memory cells, a plurality of bit lines, a plurality of control gate lines, and at least one common line, each memory cell is configurable to store one of 2^N values, where N is two or greater;

at least one memory decoder coupled to the memory arrays, each memory decoder configured to provide bias signals to selected ones of the plurality of memory cells;

a reference array operatively coupled to the memory arrays and configurable to provide reference signals used for programming and reading the selected ones of the plurality of memory cells;

a plurality of local sense amplifiers, each of said plurality of local sense amplifiers being coupled to a corresponding subset of said plurality of memory cells and being selectively coupled to said bit lines;

a plurality of global bit lines, each local sense amplifier being coupled to one of said plurality of global bitlines;

a plurality of global sense amplifiers, each global sense amplifier being coupled to a group of said global bitlines and said reference array to generate an output signal indicative of the comparison between a voltage detected in a selected memory cell and a reference signal; and

a circuit to compare the output signal from one of said global sense amplifiers corresponding to a selected memory cell and one of said reference signals from said reference array and determining whether said output signal is within a predetermined relationship of said one of said reference signals during a programming, erase or reading of said selected memory cell and setting a flag to indicate whether a predetermined relationship is determined.

65. (Original) The data storage system of claim 64 wherein said circuit reprograms said selected memory cell in the event the circuit determines said output signals within a margin of said one of said reference signals.

66. (Original) The data storage system of claim 65, wherein said circuit further compares the output signal from said one of said global sense amplifiers corresponding to said selected memory cell and another one of said reference signals from said reference array in determining whether said output signal is within another margin of said another one of said reference signals.

67. (Original) The data storage system of claim 66 wherein said circuit reprograms said selected memory cell in the event the circuit determines said output signals within a margin of said one of said reference signals.

68. (Cancelled)

69. (Original) A data storage system comprising:

a plurality of memory arrays, each memory array including a plurality of memory cells, a plurality of bit lines, a plurality of control gate lines, and at least one common line, each memory cell is configurable to store one of 2^N values, where N is two or greater;

at least one memory decoder coupled to the memory arrays, each memory decoder configured to provide bias signals to selected ones of the plurality of memory cells;

a reference array operatively coupled to the memory arrays and configurable to provide reference signals used for programming and reading the selected ones of the plurality of memory cells;

a plurality of local sense amplifiers, each of said plurality of local sense amplifiers being coupled to a corresponding subset of said plurality of memory cells and being selectively coupled to said bit lines;

a plurality of global bit lines, each local sense amplifier being coupled to one of said plurality of global bitlines;

a plurality of global sense amplifiers, each global sense amplifier being coupled to a group of said global bitlines to capacitively detect a voltage on one of said global bitlines and said reference array to capacitively detect one of said reference signals to generate an output signal indicative of the comparison between said detected voltage in a selected memory cell and a reference signal; and

a circuit to compare the output signal from one of said global sense amplifiers corresponding to a selected memory cell and one of said reference signals from said reference array and determining whether said output signal is within a predetermined relationship of said one of said reference signals during a programming, erase or reading of said selected memory cell and setting a flag to indicate whether a predetermined relationship is determined.

70. (Cancelled)

71. (Original) A data storage system comprising:

a plurality of memory arrays, each memory array including a plurality of memory cells, a plurality of bit lines, a plurality of control gate lines, and at least one common line, each memory cell is configurable to store one of 2^N values, where N is two or greater;

at least one memory decoder coupled to the memory arrays, each memory decoder configured to provide bias signals to selected ones of the plurality of memory cells;

a reference array operatively coupled to the memory arrays and configurable to provide reference signals used for programming and reading the selected ones of the plurality of memory cells;

a plurality of local sense amplifiers, each of said plurality of local sense amplifiers being coupled to a corresponding subset of said plurality of memory cells and being selectively coupled to said bit lines;

a plurality of global bit lines, each local sense amplifier being coupled to one of said plurality of global bitlines;

a plurality of global sense amplifiers, each global sense amplifier being coupled to a group of said global bitlines and said reference array to generate an output signal indicative of the comparison between a voltage detected in a selected memory cell and a reference signal, and including a circuit to equalize inputs and the output of the global sense amplifier in response to an autozero signal; and

a circuit to compare the output signal from one of said global sense amplifiers corresponding to a selected memory cell and one of said reference signals from said reference array and determining whether said output signal is within a predetermined relationship of said one of said reference signals during a programming, erase or reading of said selected memory cell and setting a flag to indicate whether a predetermined relationship is determined.

72. (Original) The data storage system of claim 71 wherein said circuit reprograms said selected memory cell in the event the circuit determines said output signals are within a margin of said one of said reference signals.

73. (Original) The data storage system of claim 71, wherein said circuit further compares the output signal from said one of said global sense amplifiers corresponding to said selected memory cell and another one of said reference signals from said reference array to determine whether said output signal is within another margin of said another one of said reference signals.

74. (Original) The data storage system of claim 73 wherein said circuit reprograms said selected memory cell in the event the circuit determines said output signal is within a margin of said one of said reference signals.

75. (Cancelled)

76. (Original) A data storage system comprising:

a plurality of memory arrays, each memory array including a plurality of memory cells, a plurality of bit lines, a plurality of control gate lines, and at least one common line, each memory cell is configurable to store one of 2^N values, where N is two or greater;

at least one memory decoder coupled to the memory arrays, each memory decoder configured to provide bias signals to selected ones of the plurality of memory cells;

a reference array operatively coupled to the memory arrays and configurable to provide reference signals used for programming and reading the selected ones of the plurality of memory cells;

a plurality of local sense amplifiers, each of said plurality of local sense amplifiers being coupled to a corresponding subset of said plurality of memory cells and being selectively coupled to said bit lines;

a plurality of global bit lines, each local sense amplifier being coupled to one of said plurality of global bitlines;

a plurality of global sense amplifiers, each global sense amplifier being coupled to a group of said global bitlines to capacitively detect a voltage on one of said global bitlines and said reference array to capacitively detect one of said reference signals to generate an output signal indicative of the comparison between said detected voltage in a selected memory cell and a reference signal; and

a circuit to compare the output signal from one of said global sense amplifiers corresponding to a selected memory cell and one of said reference signals from said reference array and determining whether said output signal is within a predetermined relationship of said one of said reference signals during programming, erasing or reading of said selected memory cell and setting a flag to indicate whether a predetermined relationship is determined.

77. (Original) A data storage system comprising:

a plurality of memory arrays, each memory array including a plurality of memory cells, a plurality of bit lines, a plurality of control gate lines, and at least one common line, each memory cell is configurable to store one of 2^N values, where N is two or greater;

at least one memory decoder coupled to the memory arrays, each memory decoder configured to provide bias signals to selected ones of the plurality of memory cells;

a reference array operatively coupled to the memory arrays and configurable to provide reference signals used for programming and reading the selected ones of the plurality of memory cells;

a plurality of local sense amplifiers, each of said plurality of local sense amplifiers being coupled to a corresponding subset of said plurality of memory cells and being selectively coupled to said bit lines;

a plurality of global bit lines, each local sense amplifier being coupled to one of said plurality of global bitlines;

a plurality of global sense amplifiers, each global sense amplifier being coupled to a group of said global bitlines and said reference array to generate an output signal indicative of the comparison between a voltage detected in a selected memory cell and a reference signal and including a circuit to equalize inputs and the output of the global sense amplifier in response to an autozero signal; and

a circuit to compare the output signal from one of said global sense amplifiers corresponding to a selected memory cell and one of said reference signals from said reference array and determining whether said output signal is within a predetermined relationship of said one of said reference signals during a programming, erase or reading of said selected memory cell and setting a flag to indicate whether a predetermined relationship is determined.

78. (Original) A data storage system comprising:

a plurality of memory arrays, each memory array including a plurality of memory cells, a plurality of bit lines, a plurality of control gate lines, and at least one common line, each memory cell is configurable to store one of 2^N values, where N is two or greater, the memory cell being programmed in response to a shaped program pulse applied to said at least one common line;

at least one memory decoder coupled to the memory arrays, each memory decoder configured to provide bias signals to selected ones of the plurality of memory cells;

a reference array operatively coupled to the memory arrays and configurable to provide reference signals used for programming and reading the selected ones of the plurality of memory cells;

a plurality of local sense amplifiers, each of said plurality of local sense amplifiers being coupled to a corresponding subset of said plurality of memory cells and being selectively coupled to said bit lines;

a plurality of global bit lines, each local sense amplifier being coupled to one of said plurality of global bitlines; and

a plurality of global sense amplifiers, each global sense amplifier being coupled to a group of said global bitlines and said reference array to generate an output signal indicative of the comparison between a voltage detected in a selected memory cell and a reference signal.

79. (Original) The data storage system of claim 78 wherein said shaped program pulse has a two-step ramp rate.

80. (Cancelled)

81. (Original) A data storage system comprising:

a plurality of memory arrays, each memory array including a plurality of memory cells, a plurality of bit lines, a plurality of control gate lines, and at least one common line, each memory cell is configurable to store one of 2^N values, where N is two or greater, the memory cell being programmed in response to a shaped program pulse applied to said at least one common line;

at least one memory decoder coupled to the memory arrays, each memory decoder configured to provide bias signals to selected ones of the plurality of memory cells;

a reference array operatively coupled to the memory arrays and configurable to provide reference signals used for programming and reading the selected ones of the plurality of memory cells;

a plurality of local sense amplifiers, each of said plurality of local sense amplifiers being coupled to a corresponding subset of said plurality of memory cells and being selectively coupled to said bit lines;

a plurality of global bit lines, each local sense amplifier being coupled to one of said plurality of global bitlines; and

a plurality of global sense amplifiers, each global sense amplifier being coupled to a group of said global bitlines to capacitively detect a voltage on one of said global bitlines and said reference array to capacitively detect one of said reference signals to generate an output signal indicative of the comparison between said detected voltage in a selected memory cell and a reference signal.

82. (Original) The data storage system of claim 81, wherein the shaped program pulse has a two-step ramp rate.

83. (Original) The data storage system of claim 81 wherein the ramp rate is programmable.

84. (Cancelled)

85. (Original) A data storage system comprising:

a plurality of memory arrays, each memory array including a plurality of memory cells, a plurality of bit lines, a plurality of control gate lines, and at least one common line, each memory

cell is configurable to store one of 2^N values, where N is two or greater, the memory cell being programmed in response to a shaped program pulse applied to said at least one common line;

at least one memory decoder coupled to the memory arrays, each memory decoder configured to provide bias signals to selected ones of the plurality of memory cells;

a reference array operatively coupled to the memory arrays and configurable to provide reference signals used for programming and reading the selected ones of the plurality of memory cells;

a plurality of local sense amplifiers, each of said plurality of local sense amplifiers being coupled to a corresponding subset of said plurality of memory cells and being selectively coupled to said bit lines;

a plurality of global bit lines, each local sense amplifier being coupled to one of said plurality of global bitlines; and

a plurality of global sense amplifiers, each global sense amplifier being coupled to a group of said global bitlines and said reference array to generate an output signal indicative of the comparison between a voltage detected in a selected memory cell and a reference signal and including a circuit to equalize inputs and the output of the global sense amplifier in response to an autozero signal.

86. (Original) The data storage system of claim 85, wherein the shaped program pulse has a two-step ramp rate.

87. (Original) The data storage system of claim 85, wherein the ramp rate is programmable.

88-126. (Cancelled)